REMARKS

The Office Action of August 23, 2006 has been received and its contents carefully considered. A Request for Continued Examination (RCE) is being filed concurrently in order to permit further prosecution.

The present Amendment revises independent claims 1 and 7 to recite further features of the "parallel/serial conversion circuit." The revisions are supported (for example) by Figure 1 of the application's drawings. As will be seen from Figure 1, a selector 52 in the parallel/serial conversion circuit 50 receives the clock signal CK and selectively outputs data from the last scan registers 24 and 28 in response to the clock signal CK. In addition, a flip-flop 53 latches the output data from the selector 52 in response to the multiplied clock signal CKD.

For the reasons discussed below, it is respectfully submitted that the inventions defined by the current formulation of the independent claims are patentable over the cited references. While it is believed that previous arguments that have been advanced remain valid, despite the comments in the "Response to Amendment" section on pages 2-4 of the Office Action, the following remarks will primarily address the references with respect to the new claim language.

Figure 8 of the Whetsel reference shows scan collectors PSC that receive the output of scan paths. The reference does not explicitly disclose the circuitry in these scan collectors. However, the reference states, with regard to a previously-described embodiment, that scan collector circuits in the previous embodiment "are basically

parallel-input serial-output shift registers" (column 3, lines 59-62). There is no suggestion in Whetsel of a parallel/serial conversion circuit which comprises a selector that receives a clock signal and a flip-flop that latches the output from the selector in response to a multiplied clock signal.

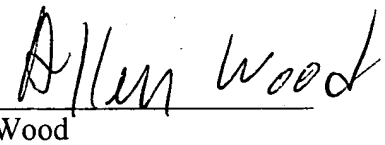
The Eriksson et al reference (hereafter simply "Eriksson") discloses a parallel/serial converter (in addition to a serial-parallel converter), but Eriksson neither discloses nor suggests a parallel/serial converter that includes a selector that receives a clock signal and a flip-flop that receives a multiplied clock signal. Accordingly, even if an ordinarily skilled person thought that it might be desirable for some reason to replace Whetsel's scan collectors with parallel/serial converters in accordance with Eriksson, the result would still not be what is recited in the independent claims.

The Kobayashi reference discloses a scan output conversion circuit 11 that receives inputs from four scan chains and converts them into an 8-bit output. Kobayashi's circuit 11 is therefore more in the nature of the serial/parallel converter than a parallel/serial converter. The details of Kobayashi's scan output conversion circuits are shown in Figures 4 and 9 of the reference, and it is respectfully submitted that Kobayashi's scan output conversion circuits would not have led an ordinarily skilled person to modify Whetsel/Eriksson so as to achieve what is now recited in independent claims 1 and 7.

The remaining claims depend from the independent claims discussed above and recited additional limitations to further define the invention, so they are patentable along with their independent claims and need not be further addressed.

For the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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